Ensuring signal integrity in high-speed connectors

Channel characterization has become a major signal integrity issue, requiring manufacturers to develop test methods that will ensure that devices perform as specified.

by **Markus Witte**

THE NEED for speed is everywhere. Internet Protocol (IP) has become tremendously important for combining data, voice and video in the same data stream. Different networks, like IMS (Internet Protocol Multimedia Subsystem), VoIP (Voice-over-Internet Protocol), Mobile VoIP, and others use the same protocol for these data packages—referred to as converging networks. Mobile data services require a higher aggregate

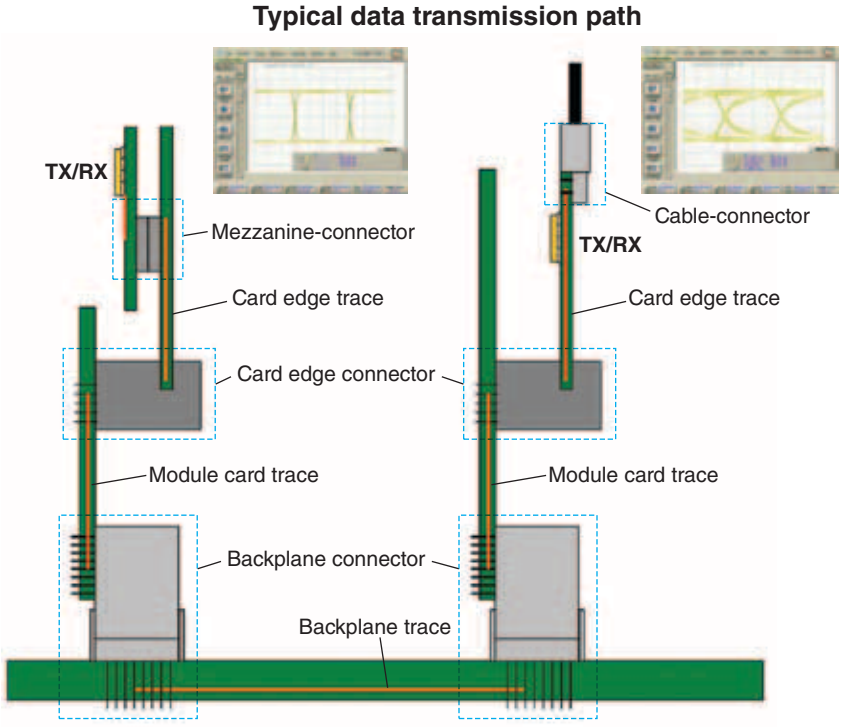

FIGURE 1. *Signal transmission between transmitter and receiver can be from chip-to-chip on the same board, or chip-to-chip between different boards. In this illustration, the data transmission path shows an assignment of different connectors.*

bandwidth for network elements like base stations, radio network controllers and core networks, which have to accommodate this increased data traffic.

What started as a gradual trend to higher bit rates accelerated dramatically in 2004 with the introduction by Intel of the PCI Express standard. Following Intel's lead, the majority of chip-to-chip connection standards underwent an architectural shift from parallel busses to serializer/deserializer (SERDES) links, called "lanes."

With the IP-based infrastructure, new standards, such as IEEE 802.3ap, evolved for higher data rates—especially for Ethernet over the backplane assembly. Other standards, such as RapidIO, also address higher data rates that typically are in the range of 3.125 Gigabaud (Gbd) per lane—and some interconnects already support 10.3125 Gbd lane rates. Different protocols are used for the data transport, and each link technology has different requirements for the channel; however, some limits and electrical requirements are defined in the relevant specification.

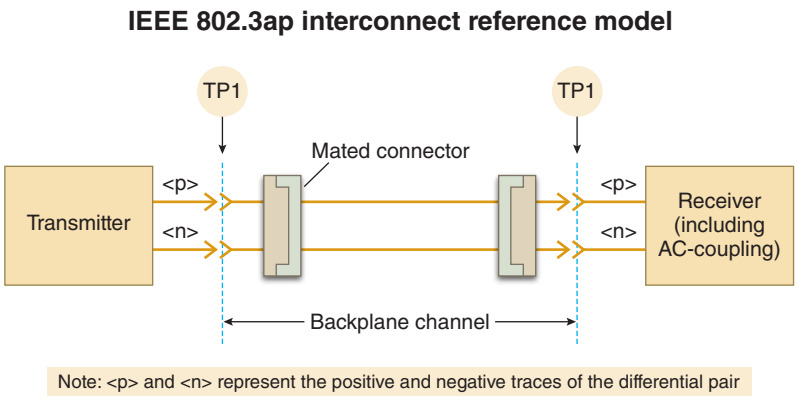

FIGURE 2. *In IEEE 802.3ap, TP1 and TP4 are reference test points, with the backplane channel in between.*

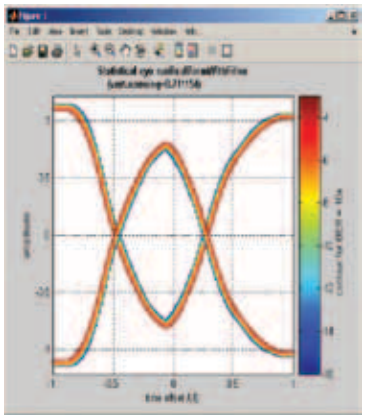

FIGURE 3. *While a Stateye tool has been used to run compliance testing for some high-speed connector standards, the results do not guarantee that the channel will work without bit error rates.*

Even while IEEE 802.3ap is being used for new backplane designs, the Ethernet task force is developing IEEE 802.3ba for 40 and 100Gbits/sec in future data networks. Meanwhile, AdvancedTCA (Advanced Telecommunications Computing Architecture) is the largest specification effort in the history of the PCI Industrial Computer Manufacturers Group (PICMG), which is targeted to requirements for the next generation of "carrier grade" communications equipment. This series

of specifications incorporates the latest trends in high-speed interconnect technologies and next-generation processors, promising improved reliability and availability.

But these advantages of larger increases in bit rate come at a cost. At multi-gigabit per second data rates, with channel flight times longer than a bit period, signal integrity is compromised. High-speed analog effects can impair the signal quality and degrade the bit error rate (BER) of the link.

To ensure optimum performance of high-speed connectors, manufacturers need to perform simulation and characterization analysis—comprehensive and empirical—in order to establish and adhere to uniform standards.

Channel characterization

Signal integrity studies the design of high-speed circuits and the accommodation of cleaner signals passing through them. Cleaner signals enable engineers to identify and minimize sources of distortion in data transmission, which could otherwise disrupt timing of the digital logic.

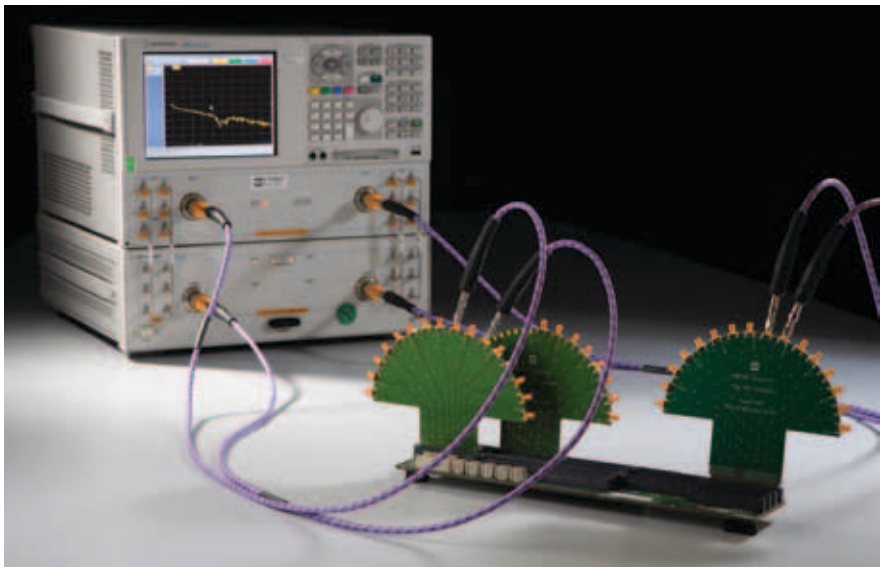

FIGURE 4. *A high-precision probe station can be used to avoid rise time degradations and reflections from the launch connector transition.*

The ability to effectively transmit a signal is related to the ratio of signal to interference that is presented to the receiver. Many challenges must be addressed in developing a system in which any channel can support transmission of a signal serially at 10 Gbits/sec. At multi-gigabit/sec data rates, link designers must consider reflections at impedance changes, noise induced by densely packed neighboring connections (crosstalk), and high-frequency attenuation. Other significant issues of concern for signal integrity that can plague modern digital products and interfere with the detection of the output

signal include ringing, ground bounce, and power supply noise.

Harting has conducted comprehensive signal integrity tests of connectors in backplane applications, as have supporting sub-standardization committees within PICMG and OBSAI (Open Base Station Architecture Initiative). Standards like IEEE 802.3ap have become relevant, and appendix 69B defines the informative limits of the channel. While a confidence level is defined, this is neither normative nor a guarantee that the channel will work without a BER failure.

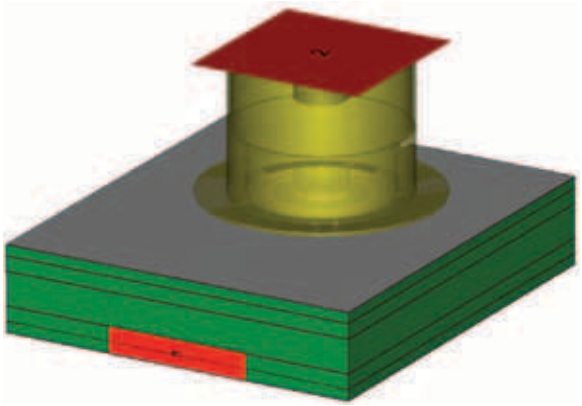

FIGURE 5. *In this SMA termination, transition from the board-mount coax connector to the PCB trace is optimized with a 3D dynamic field solution.*

Obviously, it is challenging to define normative parameters, especially for lane rates beyond 3.125 Gbd, due to the need of signal conditioning. The separation of the channel with defined reference points helps to isolate specific areas of the transmission path; however, cascading the signal elements later requires careful calibration and de-embedding techniques, especially between the reference transition points.

The PICMG ICCC (Interconnect Channel Characterization Committee) has been challenged to develop a document with ground rules and definitions for channel characterization. To take it a step further and consider the signal propagation path from the cable connector, it becomes even more difficult. For example, 10 Gbit/sec Small Form Factor Pluggable (SFP+) modules and hosts are well defined within the latest SFF draft specifications, with specific electrical requirements and test procedures. While focusing mainly on the physical layer, the transmission of signals between transmitter and receiver can be from chip-to-chip on the same board or chip-to-chip between different boards. When the signal is between different boards, the physical connection could be a PCB, cable, or connector.

Figure 1 illustrates a data transmission path with an arbitrary assignment of different connector types.

PCB and cable signal traces carry much more current than the iron-chip counterparts. This larger current induces crosstalk, primarily in a magnetic

or inductive mode, as opposed to a capacitive mode. To combat this crosstalk, digital PCB designers must remain acutely aware of the intended signal path for every signal, as well as the path of returning signal current for every signal. The signal itself and its returning signal current path are equally capable of generating inductive crosstalk.

Measurement of the signal between the chips is not trivial and the test fixture and measurement procedure will have a strong impact on the results. Therefore, a comprehensive documentation with all details of the test fixture and instrument settings is mandatory for the interpretation, reproducibility, and comparison of the results.

Channel test, simulation

The backplane channel in IEEE 802.3ap is defined between transmitter and receiver test points TP1 and TP4. While TP1 and TP4 are reference test points (Figure 2), informative channel parameters between these points are defined in Annex 69B for 1000Base-KX @1.25 Gbd, 10GBase-KX4 @3.125 Gbd, and 10GBase-KR @10.3125 GBd:

:: Characteristic impedance;

:: Fitted attenuation;

:: Insertion loss;

:: Insertion loss deviation;

:: Return loss;

:: Crosstalk;

:: Power sum differential near-end crosstalk (PSNEXT);

:: Power sum differential far-end crosstalk (PSFEXT);

:: Power sum differential crosstalk;

:: Insertion loss to crosstalk ratio (ICR).

At these new multi-gigabit/sec bit rates, the bit period is shorter than the flight time, and echoes of previous pulses can arrive at the receiver on top of the main pulse and corrupt it. In signal integrity engineering, this is called an eye closure—a reference to the clutter in the center of a type of oscilloscope trace, called an eye diagram—representing the results of a simulation driven

by a long, multi-cycle sequence that superimposes each bit period over the top of others.

In IEEE 802.3ap, the test parameters are informative only and the results do not guarantee that the channel finally works without bit error rates. While other standards, like RapidIO or the OIF-CEI02.0 agreement, use tools like Stateye for compliance testing, correct measurement of the data is a vital concern for manufacturers.

Characterization of the passive channel is not trivial. Data transmission through the channel (Figure 1) is very complicated. The measurement instrument's cables are terminated with coax connector types like 2.4-mm/2.92-mm/3.5-mm. Access to the component edges is difficult, so four measurement test fixtures are needed. The test fixture has a strong impact on the results. An error correction is required to remove these effects from the measurement data. To avoid the rise time degradations and reflections due to the launch connector transition, use of a high-precision probe (ProbeStation) is recommended.

At multi-gigabit per second data rates, with channel flight times longer than a bit period, signal integrity is compromised. High-speed analog effects can impair the signal quality and degrade the bit error rate (BER) of the link.

Launch of the connectors for the instrument cables (most likely SMA termination) to the PCB must be very smooth. The transition from the board-mount coax connector to the PCB trace is optimized with a 3D dynamic field solver. The production process of the test cards is very critical. In particular, the impedance match of the test fixture, including the connector transition, has to be very accurate.

Scattering (S)-Parameters are measured with a Multiport Vector Network Analyzer. S-Parameters can capture the reflection and transmission from junctions in backplanes. Further, the isolation between signals is important to control for avoiding interferences caused by adjacent channels.

The data can also be gained with a time domain instrument, though a transformation from the time domain into the frequency domain is required.

The selection of the best suitable software tools and measurement equipment is important to do the channel characterization; however, the skills required for properly using the software and test equipment is the biggest key for accurate results.

High-speed design

As systems are developed to continually support higher-speed capacities, the design, simulation, measurement and analysis of connectors to optimize channel signal integrity will need to be even more exacting.

Requirements demanded of high frequency and high-speed connections are considerable. Connections must be compact, able to withstand hard mechanical knocks, compensate for tolerances between the daughter card and the backplane while not causing significant signal reflections and signal attenuation, and must guarantee a reliable contact for at least 15 years.

Such tried and tested connection standards should be expected, and demanded, by both component manufacturers and those that integrate them. Only in this way can a truly functional mega-gigabit system that supports computing, storage, control, media, and packets become widely functional.

Markus Witte is signal integrity manager within Harting Technology Group and responsible for system and application management. He has authored and co-authored technical papers for DesignCon, and is supporting sub-standardization groups within PICMG and OBSAI.